UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	**2666.42**
First Named Inventor or Application Identifier	**YAT-TUNG LAM**
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] Fee Transmittal Form (Submit an original, and a duplicate for fee processing)
2. [X] Applicant claims small entity status. See 37 CFR 1.27.
3. [X] Specification — *Total Pages* 36
4. [X] Drawing(s) *(35 USC 113)* — *Total Sheets* 6
5. [X] Oath or Declaration — *Total Pages* 2
   - a. [X] Newly executed (original or copy)
   - b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 6 below]***
     - i. [ ] DELETION OF INVENTOR(S) Signed Statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. [X] Application Data Sheet. See 37 CFR 1.76

See attached.

This application claims priority from U.S. Patent Appln. No. 60/217,418, filed July 11, 2000.

7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. [ ] Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Form (CRF)
   - b. Specification Sequence Listing on:
     - i. [ ] CD-ROM or CD-R (2 copies); or
     - ii. [ ] paper
   - c. [ ] Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. [X] Assignment Papers (cover sheet & document(s))
10. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
11. [ ] English Translation Document *(if applicable)*
12. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
13. [ ] Preliminary Amendment
14. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other: _____

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No. __/_____

Prior application information: *Examiner* _____ *Group/Art Unit:* _____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

18. CORRESPONDENCE ADDRESS

[X] Customer Number or Bar Code Label 05514 (Insert Customer No. or Attach bar code label here) or [ ] Correspondence address below

NAME					
Address					
City		State		Zip Code	
Country		Telephone		Fax	

CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS (37 CFR 1.16(c))	50 -20 =	30	X $ 18.00 =	$540.00
	INDEPENDENT CLAIMS (37 CFR 1.16(b))	20 -3 =	17	X $ 80.00 =	$1,360.00
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.16(d))			$270.00 =	$270.00
				BASIC FEE (37 CFR 1.16(a))	$710.00
			Total of above Calculations =		$2,880.00
	Reduction by 50% for filing by small entity (Note 37 CFR 1.9, 1.27, 1.28).				$1,440.00
				TOTAL =	$1,440.00

19. Small entity status

a. [X] A small entity statement is enclosed

b. [ ] A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.

c. [ ] Is no longer claimed.

20. [X] A check in the amount of $ 1,440.00 to cover the filing fee is enclosed.

21. [X] Two (2) checks in the amount of $ 40.00 each to cover the recordal fee are enclosed.

22. The Commissioner is hereby authorized to credit overpayments or charge the following fees to Deposit Account No. 06-1205:

a. [X] Fees required under 37 CFR 1.16.

b. [X] Fees required under 37 CFR 1.17.

c. [ ] Fees required under 37 CFR 1.18.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED	
NAME	**RICHARD P. BAUER, REG. NO. 31,588**
SIGNATURE	
DATE	**October 4, 2000**

Applicant, Patentee, or Identifier: YAT-TUNG LAM
Application or Patent No.: Not Yet Assigned
Filed or Issued: Concurrently Herewith
For: MOVABLE TAP FINITE IMPUILSE RESPONSE FILTER

Attorney's Docket No.: 2666.42

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) and 1.27(c) - SMALL BUSINESS CONCERN

I hereby declare that I am

[ ] the owner of the small business concern identified below:

[X] an official of the small business concern empowered to act on behalf of the concern identified below

NAME OF CONCERN: Marvell Technology Group, LTD
ADDRESS OF CONCERN: *Richmond House, 3rd Floor, 12 Parla Ville Road, Hamilton HM DX, Bermuda*

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled MOVABLE TAP FINITE IMPULSE RESPONSE FILTER by inventor YAT-TUNG LAM in

[X] the specification filed herewith with the title listed above.

[ ] application no. _____ filed _____.

[ ] patent no. _____, issued _____.

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

[X] No such person, concern or organization exists.

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING: Eric B. Janofsky

ADDRESS OF PERSON SIGNING: 645 Almanor Avenue, Sunnyvale, California 94086

SIGNATURE: _____ DATE: 10/3/00

INVENTOR INFORMATION

Inventor One Given Name: YAT-TUNG
Family Name: LAM
State or Province of Residence: Palo Alto, CA
Country of Residence: USA
Citizenship Country: Hong Kong

CORRESPONDENCE INFORMATION

Correspondence Customer Number: 05514
Fax: (212) 218-2200

APPLICATION INFORMATION

Title Line One: MOVABLE TAP FINITE IMPULSE RESPONSE FILTER

Total Drawing Sheets: 6
Formal Drawings?: Yes
Application Type: Utility
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Secrecy Order in Parent Appl.?: No

REPRESENTATIVE INFORMATION

Representative Customer Number: 05514

PRIOR FOREIGN OR US APPLICATIONS

Provisional Application No.: 60/217,418
Filing Date: 7-11-00
Country: US
Priority Claimed: Yes

Patent Application Data Sheet

MOVABLE TAP FINITE IMPULSE RESPONSE FILTER

BACKGROUND OF THE INVENTION

Field Of The Invention

The present invention relates to a finite impulse response filter, and particularly to such a filter in which a delay in a portion thereof has an adjustable or selectable delay period, and to an echo canceller and an Ethernet transceiver including such an FIR filter.

Description Of The Related Art

Finite impulse response (FIR) filters are extremely versatile digital signal processors that are used to shape and otherwise to filter an input signal so as to obtain an output signal with desired characteristics. FIR filters may be used in such diverse fields as Ethernet transceivers, read circuits for disk drives, ghost cancellation in broadcast and cable TV transmission, channel equalization for communication in magnetic recording, echo cancellation, estimation/prediction for speech processing, adaptive noise cancellation, etc. For example, see U.S. Patent Nos. 5,535,150; 5,777,910; and 6,035,320, the contents of each of which are incorporated herein by reference. Reference is also made to the following publications: "An adaptive Multiple Echo Canceller for Slowly Time Varying Echo Paths," by Yip and Etter, IEEE Transactions on Communications, October 1990; "Digital Signal Processing", Alan V. Oppenheim, et al., pp. 155-163; "A 100MHz Output Rate Analog-to-Digital Interface for PRML Magnetic-Disk Read Channels in 1.2um CMOS", Gregory T. Uehara and Paul R. Gray, ISSCC94/Session 17/Disk-Drive

Electronics/ Paper FA 17.3, 1994 IEEE International Solid-State Circuits Conference, pp. 280-281; "72Mb/S PRML Disk-Drive Channel Chip with an Analog Sampled Data Signal Processor", Richard G. Yamasaki, et al., ISSCC94/Session 17/Disk-Drive Electronics/Paper FA 17.2, 1994 IEEE International Solid-State Circuits Conference, pp. 278, 279; "A Discrete-Time Analog Signal Processor for Disk Read Channels", Ramon Gomez, et al., ISSCC 93/Session 13/Hard Disk and Tape Drives/Paper FA 13.1, 1993 ISSCC Slide Supplement, pp. 162, 163, 279, 280; and "A 50MHz 70 mW 8-Tap Adaptive Equalizer/Viterbi Sequence Detector in 1.2 um CMOS", Gregory T. Uehara, et al. 1994 IEEE Custom Integrated Circuits Conference, pp. 51-54, the contents of each being incorporated herein by reference.

Typically, an FIR filter is constructed in multiple stages, with each stage including an input, a multiplier for multiplication of the input signal by a coefficient, and a summer for summing the multiplication result with the output from an adjacent stage. The coefficients are selected by the designer so as to achieve the filtering and output characteristics desired in the output signal. These coefficients (or filter tap weights) are often varied, and can be determined from a least mean square (LMS) algorithm based on gradient optimization. The input signal is a discrete time sequence which may be analog or digital, while the output is also a discrete time sequence which is the convolution of the input sequence and the filter impulse response, as determined by the coefficients.

With such a construction, it can be shown mathematically and experimentally that virtually any linear system response can be modeled as an FIR response,

as long as sufficient stages are provided. Because of this feature, and the high stability of FIR filters, such filters have found widespread popularity and are used extensively.

One problem inherent in FIR filters is that each stage requires a finite area on an integrated circuit chip. Additional area is required for access to an external pin so as to supply the multiplication or weighting coefficient for that stage. In some environments, the number of stages needed to provide desired output characteristics is large. For example, in Gigabit Ethernet applications it is preferred that every 8 meters of cable length be provided with 11 stages of FIR filter. In order to cover cable lengths as long as 160 meters, 220 FIR stages should be provided. In such environments, chip area on the integrated circuit is largely monopolized by the FIR stages.

Moreover, each FIR stage requires a finite amount of power and generates a corresponding amount of heat. Particularly where a large number of stages is needed, such power requirements become excessive and require significant mechanical adaptations to dissipate the heat.

The inventors herein have recently recognized that in some environments, not all stages of an FIR contribute significantly to the output. Figure 1, for example, is a waveform showing signal amplitude versus time in an Ethernet echo cancellation application, where time (on the horizontal axis) is expressed in delay units for an FIR filter. The waveform shown in Figure 1 represents an Ethernet transmission and its echo (or, reflection). As seen in Figure 1, the waveform includes

the near end echo at region 1, followed by a relatively quiet period in region 2, a relatively negligible signal at region 3, and the far end echo at region 4. One use of an FIR filter in such an Ethernet environment is to cancel the echo so as to distinguish more clearly between incoming signals and simple reflections of transmitted signals. However, the relatively negligible signal at region 3 contributes very little to the overall output of the FIR filter. The reason for this is that, whatever value of coefficients are set at the stages corresponding to region 3, those coefficients will be multiplied by a value which is approximately zero. Thus, contributions of those signals to the FIR output will be negligible, especially compared to regions 1, 2 or 4.

The inventors have considered simplifying the selection of coefficients by setting the coefficients corresponding to region 3 to zero, which would result in simpler algorithms needed to select coefficients. However, even with zeroed coefficients, the stages corresponding to region 3 still exist on the integrated circuit chip, stealing valuable surface area and power, and generating unwanted heat.

SUMMARY OF THE INVENTION

It is an object of the present invention to address the foregoing, by providing an FIR filter in which the delay of one or more stages is selectable or adjustable with respect to the other stages.

By virtue of this arrangement, since the delay of one stage is adjustable, it is possible to "skip" areas of the input signal that are known to have negligible signal level relative to other areas of the input signal.

That is, the portion of the input signal may be delayed by a variable period before being injected into a predetermined block of FIR stages thus "skipping" over the irrelevant portions of the signal. Since the entire input signal does not need to be injected into FIR stages, fewer stages are required to filter the input signal. Moreover, since the "skipped" stages need not be fabricated on the chip, an FIR filter according to the invention ordinarily has reduced surface area, power requirements, heat generation, and taps for coefficients, relative to a prior art FIR filter in which one or more stages do not have an adjustable or selectable delay. For example, an Ethernet echo canceller that required 224 FIR stages at the prior art can now be constructed with 160 stages, i.e., 160 taps plus 64 virtual taps having a coefficient of approximately zero.

Thus, in one aspect, the invention comprises an FIR filter having multiple coefficient taps, each associated with an input signal in corresponding stages of delay from a corresponding delay element. At least one delay element has a period of delay that is selectable or adjustable independently of the period of delay for other delay elements. Preferably, the period of delay is selectable or adjustable through pin-out elements of the FIR filter. In the preferred embodiment, at power-up all delay elements in the FIR start with the same starting period of delay. Thereafter, the delay of one or more stages is adjustable with additional delay, meaning that the delay of that stage can be more, but no less than, the starting delay.

By virtue of the foregoing arrangement, in which one or more stages has a delay that is selectable or adjustable, an FIR filter according to the invention is

smaller, requires fewer pins, uses less power and generates less heat than conventional FIR filters. In particularly preferred embodiments, the FIR filter has many stages, such as 160 stages, with the delay for one or more stages being selectable to skip over relatively negligible areas of the input signal, thereby providing an FIR filter whose output performance is very close to that of an FIR filter with many more stages, such as 224 stages.

Another aspect of the invention concerns the method of selecting a delay in an FIR filter comprising multiple coefficient taps each associated with an input signal in corresponding stages of delay from a corresponding delay element in which at least one delay element has a period of delay that is selectable or adjustable independently of that of other delay elements. According to the method, delayed components of a response signal are measured, so as to identify a sequence of components that are negligibly small compared to other sequences of components. The selectable period of delay is then set to a value calculated to prevent exposure of the identified sequence to the coefficient taps. In preferred embodiments, the response signal is monitored at the beginning of the transmission of data to determine the absolute maximum value of the far end echo tap location. Preferably, the center of the far end echo of region 4 is centered on the last section of the FIR filter taps, after the delayed portion.

Because the selectable period of delay is set to a value calculated to prevent exposure of the negligible sequence of components to the coefficient taps, the selected period of delay effectively "skips" negligible periods of the filtered input signal. Preferably, the

method for selecting a period of delay is iterative, meaning that a selectable period of delay is set based on a measurement of delayed components, performance of the FIR filter is checked based on the current period of delay based on a further measurement of delayed components, and a next iterative period of delay is thereafter set based on the latest measurement of delayed components.

This brief summary has been provided so that the nature of the invention may be understood quickly. A more complete understanding of the invention can be obtained by reference to the following detailed description of the preferred embodiments in connection with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a view showing a channel response waveform over copper cable in an Ethernet environment, including near end echo and far end echo due to reflection.

Figure 2 is a functional block diagram showing an Ethernet transceiver including a transmit side and a receive side, and in which an echo canceller thereof includes an FIR filter according to the invention.

Figure 3 is a functional block diagram of the echo canceller in Figure 2, showing an FIR filter according to the invention together with least mean square elements by which the coefficient for each stage is generated, and including an adjustable delay element.

Figure 4 is a functional block diagram of the 64-delay pipe shown in Figure 3.

Figures 5a and 5b are functional block diagrams showing the FIR filter of Figure 3.

Figure 6 is a functional block diagram showing the quantizer and downsampling blocks of the FIR filter of Figure 3.

Figure 7 is a flowchart depicting a method of determining how much delay should be provided to the input signal in accordance with the present invention.

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DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

The present invention will now be described with reference with to an echo canceller used in an Ethernet transceiver device. Preferably, the echo canceller is embodied in an Integrated Circuit disposed between a digital interface and an RJ45 analog jack. The Integrated Circuit may be installed inside a PC on the network interface card or the motherboard, or may be installed inside a network switch or router. However, other embodiments include applications in read circuits for disk drives, ghost cancellation in broadcast and cable TV transmission, channel equalization for communication in magnetic recording, echo cancellation, estimation/prediction for speech processing, adaptive noise cancellation, etc. All such embodiments are included within the scope of the appended claims.

While the present invention is described with respect to a digital FIR filter, is to be understood that the structure and functions described herein are equally applicable to an analog FIR. Moreover, while the invention will be described with respect to the functional elements of the FIR filter, the person of ordinary skill in the art will be able to embody such functions in discrete digital or analog circuitry, or as software executed by a general purpose process (CPU) or digital signal processor.

A functional block diagram of an Ethernet transceiver incorporating an FIR filter according to the present invention is depicted in Figure 2. Although only one channel is depicted therein, four parallel channels are typically used in Gigabit Ethernet applications. Only one channel is depicted and described herein for clarity.

A 125 MHz, 250Mbps digital input signal from a PC is PCS-encoded in a PCS encoder 2 and is then supplied to a D/A converter 4 for transmission to the Ethernet cable 6. The PCS-encoded signal is also supplied to a NEXT (Near End Transmitter) noise canceller 8 and to adaptive echo canceller 10. The operation of the echo canceller 10 will be described later herein with respect to Figure 3.

Signals from the Ethernet cable 6 are received at adder 14 and added with correction signals supplied from baseline wander correction block 12 (which corrects for DC offset). The added signals are then converted to digital signals in the A/D converter 16, as controlled by timing and phase-lock-loop block 18. The digital signals from A/D converter 16 are supplied to delay adjustment block 20, which synchronizes the signals in accordance

with the four parallel Ethernet channels. The delay-adjusted digital signals are then added with the echo-canceled signals and the NEXT-canceled signals in adder 22.

The added signals are supplied to a Feed Forward Equalizer filter 24 which filters the signal prior to Viterbi trellis decoding in decoder 26. After Viterbi decoding, the output signal is supplied to PCS decoder 28, after which the PCS-decoded signal is supplied to the PC.

The decoder 26 also supplies output signals to a plurality of adaptation blocks schematically depicted at 30 in Figure 2. As is known, such adaptation blocks carry out corrections for such conditions as temperature offset, connector mismatch, etc. The adaptation block 30 provides output to the baseline wander correction circuit 12, the timing and phase-lock-loop circuit 18, the echo canceller 10, and the NEXT canceller 8.

Each functional block depicted in Figure 2 includes a slave state controller (not shown) for controlling the operation and timing of the corresponding block. A PCS controller 32 controls the slave state controllers of all elements depicted in Figure 2, in a manner to be described below.

Figure 3 is a functional block diagram of the echo canceller 10 shown in Figure 2. In Figure 3, the PCS-encoded logic signal is provided to logic encoder 302 as a five level logic signal (e.g. -1, -0.5, 0, +0.5, +1). The encoder 302 encodes the signal as 3 control bits, which correspond to the five logic levels of the PCS-encoded signal (e.g. -1=100; -0.5=101; 0=010; 0.5=001; 1=000). These control bits are supplied to a first

plurality or block of filter stages 304 (comprising taps 0 to 31 of the FIR filter), a second plurality or block of filter stages 306 (comprising taps 32 to 63), a third plurality or block of filter stages 308 (comprising taps 64 to 95), and a fourth plurality or block of filter stages 310 (comprising taps 96 to 127).

Filter blocks 304, 306, 308, and 310 typically have fixed delay periods between each of the taps for constant sampling of the early regions of the input signal where significant signal strength is present. Referring to Figure 1, large amplitudes are present in regions 1 and 2 of the input signal, and (according to the present embodiment) the blocks 304, 306, 308, and 310 receive these regions of the input signal to insure filtering of these significant portions of the signal. A more detailed description of the filter blocks will be provided later herein.

The logic-level-encoded signal from encoder 302 is also supplied to a 64-delay pipe (with 4 increment) 312. The delay pipe 312 is controlled by the echo controller's sequence control state machine 314 so that the portion of the input signal having the most significant echo noise is supplied to filter block 316 for noise cancellation. That is, the region 3 of the input signal is delayed appropriately in delay pipe 64 so that region number 3 is not subjected to echo cancellation (it is "skipped over") until portion 4 can be received and input into filter block 316. This way, not the entire input signal is FIR-filtered, and not as many taps are needed to effectively cancel the echo in the input signal. The method by which the signal is selectively delayed will be described in more detail below.

The output of the logic level encoder 302 is also supplied to a quantizer 318 which encodes the three control bits into two logic bits for application to downsampling blocks 322 and 324 (to be described below). For example, the quantizer 318 encodes 000 as 00; 001 as 00; 010 as 10; 101 as 01; and 100 as 01. The quantizer 318 thus performs a rounding function so that the encoded signal may be used to control the least mean squares (LMS) engines 0 through 6.

The LMS engines 4, 5, and 6 are designed to supply tap weighting coefficients to a single block of 32 FIR filter taps, and thus downsampling block 324 can use the same quantizer data for 32 cycles. In contrast, and in accordance with the present invention, LMS engines 0, 1, 2, and 3 are designed to supply tap weighting coefficients to taps 0 to 31 of filter block 304, and downsampling block 322 controls each of these LMS engines in a time-cyclic fashion. This architecture allows more precise filtering of the early regions of the input signal having significant signal strength. For example, at time t1, LMS engine 0 supplies a weighting coefficient to tap 0, LMS engine 1 supplies a weighting coefficient to tap 1, LMS engine 2 supplies a weighting coefficient to tap 2, and LMS engine 3 supplies a weighting coefficient to tap 3. At time t2, LMS engine 0 supplies a weighting coefficient to tap 1, LMS engine 1 supplies a weighting coefficient to tap 2, LMS engine 2 supplies a weighting coefficient to tap 6, and LMS engine 3 supplies a weighting coefficient to tap 4. In this cyclic fashion, LMS engines 0-3 supply weighting coefficients to more precisely filter the region 1 of the input signal, in contrast to the less precise filtering of the region 2 of the input signal filtered by filter blocks 306, 308, and 310. The above is described in more detail in commonly

assigned U.S. Patent application Serial No. 09/465228, filed December 19, 1999 and entitled, ``A Method and Apparatus for Digital Near-End Echo / Near-End Crosstalk Cancellation with Adaptive Correlation'', the contents of which is incorporated herein by reference.

The quantizer 320 quantizes the output of the delay pipe 312 and supplies it to the downsampling block 324 in a manner similar to that described above with respect to quantizer 318. Downsampling block 326 then controls LMS engine 7 which supplies weighting coefficients to the taps 128 to 159 of the filter block 316 (which thus filters the adaptively delayed portion of the input signal).

The manner by which the LMS engines generate the tap coefficients will now be described. The LMS engines 0 to 7 input error signals from the FFE 24 or the Viterbi decoder 26 of Figure 2. A memory 330 stores weighting coefficients for each of taps 32-127. As the error signal is received from the FFE 24 or the Viterbi decoder 26, the appropriate coefficients are extracted from memory 330, applied through the corresponding LMS engine, and provided to the appropriate taps 32-127 in order to filter the input signal to eliminate the echo noise in region 2 of the input signal.

In a manner similar to that described above, memory 332 stores coefficients for the taps 0-31 of the filter block 304. The appropriate coefficients are extracted from memory 332 and applied to the appropriate LMS engines 0-3 together with the error signal, and the appropriate coefficients are then supplied to the taps 0-31 to appropriately filter the echo noise in region 1 of the input signal. Similarly, the memory 334 stores

coefficients for the taps 128-159, which are selectively applied to the LMS engine 7 together with the error signal. The appropriate tap coefficients are then applied to filter block 316.

Figure 4 is a functional block diagram of the 64-delay element 312 of Figure 3. As can be seen, the 64 delay elements are grouped in sets of four delay elements 412, 414, 416, and 418. The logic level-encoded signal S is input to the delay pipe and may be delayed in increments of four by activation of control signals at gates 420, 422, and 424. The control signals are supplied by the sequence control state machine 314, and are varied in accordance with which portion of the input signal is to be skipped, as will be described below.

Figure 5a is a functional block diagram of the FIR filter showing how the variable delay D is supplied to an existing delay element 512 in order to variably adjust the input signal to skip the desired portion thereof. In Figure 5a, the logic level-encoded signal S is supplied, for example, to a first element 520 having a time delay t1. A tap coefficient C0 is applied to a multiplier 505 in order to weight the first tap of the FIR filter. The weighted signal is then provided to a summer 515 where it is added to the outputs of the other stages (to be described below), and then output as signal So. The signal S is also supplied to the multiplier 518 for multiplication by coefficient C1, and addition with the other outputs at summer 514. Of course, any number of additional stages like 520 may be provided prior to the output, as required.

The input signal S is also supplied to delay element 512 having a variable delay D. The thus-delayed

signal Svd is then provided to a series of sequential delay elements including delay element 506, which preferably also has a fixed delay time t1. The delayed signal Svd is also supplied to multiplier 516 for multiplication by coefficient Cn-2 and addition in summer 513, as shown. The output of delay element 506 Svd+t1 is supplied to both another delay element 502 (having a t1 delay) and a multiplier 510 where it is multiplied by coefficient Cn-1. The output of element 502 Svd+t1+t1 is supplied to multiplier 504 where it is multiplied by coefficient Cn and then added, in adder 508, to the output from multiplier 510. In this manner, the series of weighted tap coefficients and corresponding input signals are processed through the FIR filter, in a manner known to those of skill in the art.

The appropriate number of stages with corresponding delay elements are provided in order to properly filter the regions of the input signal having significant signal strength, such as regions 1 and 2 in Figure 1. However, to skip those insignificant portions of the signal (such as region 3), the element 512 is provided with the variable delay D in accordance with control signal Ct supplied from the sequence control state machine 314. According to the present invention, the variable delay D may be selected to skip any portion of the input signal which is not to be filtered. Preferably, a later portion of the input signal will be filtered since significant echo typically resides therein. Accordingly, after element 512, any number of additional stages like elements 502 and 506 are provided, typically having the same fixed time delay t1. The number of additional stages after stage 512 may be varied to appropriately filter the echo regions of the input signal.

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Figure 5b shows an alternative wherein the delay element 584 is provided to the undelayed portion of the input signal S to skip portions thereof. Like reference numerals represent like structure. In Figure 5b, the input signal S is supplied to both of multipliers 590 and 592 where it is respectively multiplied by coefficients C0 and C1. The delayed signal Svd output from element 584 is, after any number of intervening stages, supplied to both multipliers 510 and 504 where it is respectively multiplied by coefficients Cn-1 and Cn. The output of multiplier 504 is delayed in a delay element 502 having a t1 delay, and then supplied to adder 508 where it is added to the output from multiplier 510. The output of adder 508 is then supplied to a delay element 506 having a delay of t1, and the output of 506 is, in turn, provided (after any number of intermediate stages) to the adder 514 where it is added with the output of multiplier 590. The output of adder 514 is provided to a delay element 586 having a t1 delay. The output of the element 586 is added, in adder 588, to the output of multiplier 592, and the output of adder 588 is the output signal S0.

In a further alternative to the above arrangement, variable delays may be provided to more than one filter block. For example, filter block(s) 310 and/or 308 and/or 306 may also be supplied with variable delays so that any portions of the input signal may be skipped or filtered as the circuit designer requires. All such alternatives are included within the scope of the appended claims.

Figure 6 is a functional block diagram of the quantizer and downsampling circuits of Figure 3. The quantizer 318 receives the logical level-encoded signal S from the input of delay pipe 312. The output of quantizer

318 is provided to both the downsampling block 324 and a multiplexer 612. The multiplexer 612 outputs the quantizer signal to a one-cycle delay element 614, which supplies the down-sampled signal to LMS engine 3. In a similar manner, delay elements 616, 618, and 620 respectively provide down-sampled signals to LMS engines 2, 1, and 0, after the appropriate delay. The output of delay element 620 is also returned to the multiplexer 612, as shown.

The output of downsampling block 324 is provided to the LMS engines 6, 5, and 4, as was described above with reference to Figure 3. Also, the output of the delay pipe 312 is supplied to the quantizer 320 which supplies the downsampling block 326 and LMS engine 7, as shown.

In operation, those portions of the input signal which may be skipped by the FIR filter must first be determined. Preferably, this is done by injecting a test signal into the Ethernet cable and then receiving the return signal, such as the waveform depicted in Figure 1. However, the procedure for determining the insignificant portions of the input signal may be performed at any convenient time, such as when the Ethernet is first powered on, after any Ethernet device has been plugged into the network or unplugged from the network, during any lull in Ethernet communications, on a periodic basis, or continually. The signal used to determine the delay may also be any appropriate signal such as a test signal, a series of test signals, or by using actual Ethernet communication signals on-the-fly.

The method of determining how much delay to be supplied to the input signal in accordance with the embodiment of Figure 3 will now be described with respect

to the flow chart of Figure 7. This process is preferably carried out within the sequence control state machine 314, although any convenient processor and memory may be used. In Figure 7, when the Ethernet is first powered-up, data starts to be supplied to the Ethernet cable 6 at step S1. At step S2, the return signal is received and then filtered in the FIR filter using blocks 304, 306, 308, 310, and 316 contiguously so as to filter a continuous portion of the return signal. At step S4, it is determined which tap of taps 128-159 has received the maximum return signal strength. This tap is labeled tapmaxd. At step S5, tapmaxd is compared with the stored tapmaxs, and the tap having the maximum signal strength is then stored as the new tapmaxs. Of course, for the first determination, the initial tapmaxd will be stored as tapmaxs. In order to avoid storing unexpectedly large signal strength caused by noise, multiple looping for comparison is preferably employed. For example, if 32 taps are compared and tap 7 is identified as tapmaxs, the comparison will be repeated multiple times. Every comparison, tap 7 will be replaced with tapmacxs even though the tapmaxs is larger than tap 7, in order to avoid a lock up error.

At step S6, it is determined whether the end of the return signal has been reached. If the end of the return signal has not been reached, the process proceeds to step S7 where a 32 tap delay is applied to skip a portion of the return signal. Of course, any amount of tap delay (1 tap, 4 taps, 8 taps, 16 taps, 64 taps, etc.) may be used in any combination by the circuit designer to flexibly configure the FIR filter. The process then returns to step S4 to determine which tap of the newly-filtered signals has the maximum signal strength. Again,

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the determined tapmaxd is compared with the stored tapmaxs, and the maximum value is stored as the new tapmaxs in step S5.

One algorithm for performing steps S4, S5, S6, and S8 of Fig. 7 is as follows:

Let n = the number of stages in the FIR filter.
Let tap[i] = the ith stage of the FIR filter.
Let {tap[i]} = the coefficient value of the ith stage of the FIR filter.
Let Maxcoeff = the absolute value of the maximum coefficient value in the FIR filter.
Let m = the index of which tap coefficient is written into Maxcoeff.

At time = 0,

Maxcoeff ← {tap[0]}

m ← 0

At time = i, (where i › 0, i.e., 1, 2, 3, 4,…)

```
if (en_search)   //where en_search enables the search for Maxcoeff
        begin
                if (Maxcoeff ‹|{tap[i]}| or m =i)
                        begin
                                Maxcoeff ← |{tap[i]}|
                                m ← I
                        end
                else
                        begin
                                Maxcoeff ← Maxcoeff
                                m ← m
                        end
        end
```

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```
else
    begin
        Maxcoeff ← Maxcoeff
        m ← m
end.
```

In this iterative manner, the last filter block 316 is successively moved across the later portions of the return signal identifying which portion(s) of the return signal have the maximum signal strength. When the filter block 316 has reached the end of the return signal, step S8 is performed wherein the stored tapmaxs is set as the center tap of the filter block 316. Now, the filter block 316 will be applied to the center of the later portion of the return signal having the most significant signal strength. The required delay may be determined algorithmically or from accessing an entry from a lookup table. The delay required to so-position filter block 316 is then stored in the memory of sequence control state machine 314 so that all Ethernet signals received from the Ethernet cable 6 may be FIR-filtered in accordance with the thus-configured filter blocks to skip those portions of the signal having insignificant signal strength, while filtering the remaining signal. In such a manner, Ethernet signals typically requiring more than 220 taps for proper FIR filtration can be adequately filtered with an FIR filter having only 160 taps.

Thus, what has been described is method and apparatus for controlling an FIR filter so as to delay the input signal to skip over portions of that signal having insignificant signal strength. This allows the FIR filter

to have fewer taps, consuming less power and less space on the Integrated Circuit.

The individual components shown in outline or designated by blocks in the attached Drawings are all well-known in the FIR filtering arts, and their specific construction and operation are not critical to the operation or best mode for carrying out the invention.

While the present invention has been described with respect to what is presently considered to be the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, the invention is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims. The scope of the following claims is to be accorded the broadest interpretation so as to encompass all such modifications and equivalent structures and functions.

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WHAT IS CLAIMED IS:

1. FIR filter apparatus comprising:

an input for receiving an input signal;

an FIR filter comprising a plurality of filter stages; and

a delay coupled between two of said plurality of filter stages to delay application of the input signal to at least one of said filter stages to skip filtering a portion of the input signal.

2. Apparatus according to Claim 1, wherein the delay of said delay is adjustable.

3. Apparatus according to Claim 1, wherein the plurality of filter stages comprises a first plurality of stages and a second plurality of stages, the first plurality of stages receiving a predetermined first portion of the input signal, said delay providing a variable second portion of the input signal to said second plurality of stages.

4. Apparatus according to Claim 3, further comprising a memory storing a delay value for application to said delay.

5. Apparatus according to Claim 3, wherein said first plurality of filter stages comprises a plurality of filter blocks, each having a plurality of taps, and wherein said second plurality of stages comprises at least one filter block having a plurality of taps, and further comprising:

a first plurality of LMS engines which provide a first plurality of weighting coefficients to the taps of said plurality of filter blocks; and

a second LMS engine which provides a second plurality of weighting coefficients to the taps of said at least one filter block.

6. Apparatus according to Claim 5, wherein said plurality of filter blocks comprises four filter blocks each having 32 taps, and wherein said at least one filter block comprises one filter block having 32 taps.

7. FIR filter apparatus comprising:

a signal input receiving an input signal;

a first block of filter stages having a respective first plurality of taps which receive a respective first plurality of weighting coefficients, for filtering a first portion of the input signal in accordance with the first plurality of weighting coefficients;

a second block of filter stages having a respective second plurality of taps which receive a respective second plurality of weighting coefficients, for filtering a second portion of the input signal in accordance with the second plurality of weighting coefficients; and

a delay which variably delays application of the second portion of the input signal to the second block of filter stages with respect to the first portion of the input signal.

8. An FIR filter comprising:

a plurality of delay elements; and

a plurality of coefficient taps, each associated with a portion of an input signal in corresponding stages of delay from a corresponding delay element,

wherein at least one delay element has a period of delay that is selectable.

9. An FIR filter according to Claim 8, wherein the selectable period of delay is selectable independently of a period of delay for other delay elements.

10. An FIR filter according to Claim 9, wherein each delay element has a minimum period of delay, and wherein the selectable period of delay is adjustable to be greater than the minimum period of delay.

11. An FIR filter according to Claim 8, wherein the FIR filter further includes pin-out arrangements for setting the selectable period of delay.

12. FIR filter apparatus comprising:

input means for receiving an input signal;

filter means for filtering the input signal and having a plurality of filter stages; and

delay means coupled between two of said plurality of filter stages for delaying application of the input signal to at least one of said filter stages to skip filtering a portion of the input signal.

13. FIR filter apparatus comprising:

signal input means for receiving an input signal;

a first block of filter means, having a respective first plurality of taps which receive a respective first plurality of weighting coefficients, for filtering a first portion of the input signal in accordance with the first plurality of weighting coefficients;

a second block of filter means, having a respective second plurality of taps which receive a respective second plurality of weighting coefficients, for

filtering a second portion of the input signal in accordance with the second plurality of weighting coefficients; and

delay means for adjustably delaying application of the second portion of the input signal to the second block of filter means with respect to the first portion of the input signal.

14. An echo canceller comprising:

an input for receiving an input signal having an echo;

an FIR filter including:

(i) a first plurality of filter stages comprising a plurality of filter blocks, each having a plurality of taps; and

(ii) a second plurality of stages comprising at least one filter block having a plurality of taps;

a first plurality of LMS engines which provide a first plurality of weighting coefficients to the taps of said plurality of filter blocks;

a second LMS engine which provides a second plurality of weighting coefficients to the taps of said at least one filter block to filter said echo; and

a delay coupled between said plurality of filter blocks and said at least on filter block to delay application of the input signal to said at least one filter block to skip filtering a portion of the input signal which contains negligible echo.

15. An Ethernet transceiver, comprising:

an input for inputting an input signal into an Ethernet cable;

an output for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal and having an echo;

an FIR filter including:

(i) a first plurality of filter stages comprising a plurality of filter blocks, each having a plurality of taps; and

(ii) a second plurality of stages comprising at least one filter block having a plurality of taps;

a first plurality of LMS engines which provide a first plurality of weighting coefficients to the taps of said plurality of filter blocks;

a second LMS engine which provides a second plurality of weighting coefficients to the taps of said at least one filter block to filter said echo; and

a delay coupled between said plurality of filter blocks and said at least on filter block to delay application of the output signal to said at least one filter block to skip filtering a portion of the output signal which contains negligible echo.

16. A transceiver according to Claim 15, wherein said first plurality of LMS engines includes:

a first set of LMS engines applying weighting coefficients to a first filter block; and

a second set of LMS engines respectively applying weighting coefficients to a corresponding number of filter blocks.

17. A method for controlling an FIR filter comprising the steps of:

receiving an input signal;

filtering the input signal with an FIR filter having a plurality of filter stages; and

delaying application of the input signal to at least one of said filter stages with respect to the other filter stages to skip filtering a portion of the input signal.

18. A method of controlling an FIR filter comprising the steps of:

receiving an input signal;

filtering a first portion of the input signal with a first block of filter stages having a respective first plurality of taps which receive a respective first plurality of weighting coefficients, the first portion of the input signal being filtered in accordance with the first plurality of weighting coefficients;

filtering a second portion of the input signal with a second block of filter stages having a respective second plurality of taps which receive a respective second plurality of weighting coefficients, the second portion of the input signal being filtered in accordance with the second plurality of weighting coefficients; and

adjustably delaying application of the second portion of the input signal to the second block of filter stages with respect to the first portion of the input signal.

19. A method for selecting a period of delay in an FIR filter having (i) a plurality of delay elements and (ii) a plurality of coefficient taps each associated with a portion of an input signal in corresponding stages of delay from a corresponding delay element, in which at least one delay element has a period of delay that is selectable, the method comprising the steps of:

measuring components of an input signal so as to identify a sequence of components that are smaller than another sequence of larger components; and

setting the selectable period of delay to prevent application of the identified sequence of smaller components of the input signal to the coefficient taps.

20. A method according to Claim 19, further comprising the step of transmitting a test signal, wherein the input signal comprises an echo of the test signal.

21. A method according to Claim 19, wherein said steps of measuring and setting are applied iteratively with a different setting for the selectable period of delay so as to identify the sequence of smaller components.

22. FIR filter apparatus comprising:

an input responsive to an input signal;

an FIR filter comprising three filter stages; and

a first delay circuit having a first time delay coupled between two of said three filter stages;

a second delay circuit having a second time delay coupled between another two of said three filter stages, wherein the first time delay and second time delay are different.

23. An apparatus according to Claim 22, wherein the second time delay of said second delay circuit is adjustable.

24. An apparatus according to Claim 22, further comprising a selector in communication with said second delay circuit to adjust the second time delay.

25. FIR filter apparatus comprising:

a first plurality of stages serially arranged;

a delay circuit having a predetermined time delay responsive to an output of said first plurality of stages;

a second plurality of stages serially arranged and responsive to said delay circuit; and

a selector in communication with said delay circuit to adjust the predetermined time delay.

26. An apparatus according to Claim 25,

wherein the first plurality of stages are arranged in a plurality of groups, wherein each of said plurality of groups comprises at least one of said first plurality of stages, and

wherein said apparatus comprises a plurality of LMS engines, each of said plurality of LMS engines corresponding to each of plurality of groups to provide weighting coefficients.

27. An apparatus according to Claim 26,

wherein one of said plurality of groups is arranged in plural subgroups, and

wherein one of the plurality of LMS engines corresponding to said one of said plurality of groups comprises at least one LMS engine each corresponding to each one of said plural subgroups to provide weighting coefficients.

28. An echo canceller comprising:

an input for receiving an input signal;

an FIR filter including:

a first plurality of stages serially arranged;

a delay circuit having a predetermined time delay responsive to an output of said first plurality of stages;

a second plurality of stages serially arranged and responsive to said delay circuit; and

a selector in communication with said delay circuit to adjust the predetermined time delay.

29. An echo canceller according to Claim 28,

wherein the first plurality of stages are arranged in a plurality of groups, wherein each of said plurality of groups comprises at least one of said first plurality of stages, and

wherein said apparatus comprises a plurality of LMS engines, each of said plurality of LMS engines corresponding to each of plurality of groups to provide weighting coefficients.

30. An echo canceller according to Claim 28,

wherein one of said plurality of groups is arranged in plural subgroups, and

wherein one of the plurality of LMS engines corresponding to said one of said plurality of groups comprises at least one LMS engine each corresponding to each one of said plural subgroups to provide weighting coefficients.

31. An Ethernet transceiver, comprising:

an Ethernet signal input;

an Ethernet signal output; and

an FIR filter including:

a first plurality of stages serially arranged;

a delay circuit having a predetermined time delay responsive to an output of said first plurality of stages;

a second plurality of stages serially arranged and responsive to said delay circuit; and

a selector in communication with said delay circuit to adjust the predetermined time delay.

32. An Ethernet transceiver according to Claim 31,

wherein the first plurality of stages are arranged in a plurality of groups, wherein each of said plurality of groups comprises at least one of said first plurality of stages, and

wherein said apparatus comprises a plurality of LMS engines, each of said plurality of LMS engines corresponding to each of plurality of groups to provide weighting coefficients.

33. An Ethernet transceiver according to Claim 31,

wherein one of said plurality of groups is arranged in plural subgroups, and

wherein one of the plurality of LMS engines corresponding to said one of said plurality of groups comprises at least one LMS engine each corresponding to each one of said plural subgroups to provide weighting coefficients.

34. FIR filter apparatus comprising:

input means for receiving an input signal;

FIR filter means for filtering the input signal received by said input means comprising three filter stages; and

first delay means for delaying a signal between two of said three filter stages by a first time delay;

second delay means for delaying a signal between another two of said three filter stages by a second time delay, wherein the first time delay and second time delay are different.

35. An apparatus according to Claim 34, wherein the second time delay of said second delay means is adjustable.

36. FIR filter apparatus comprising:

a first plurality of filter means for filtering a signal serially arranged;

delay means for delaying an output of said first plurality of filter means by a predetermined time delay;

a second plurality of filter means for filtering a signal from said delay means; and

selector means for adjusting the predetermined time delay.

37. An apparatus according to Claim 36,

wherein the first plurality of filter means are arranged in a plurality of groups, wherein each of said plurality of groups comprises at least one of said first plurality of stages, and

wherein said apparatus comprises a plurality of LMS means, each of said plurality of LMS means corresponding to each of plurality of groups for providing weighting coefficients.

38. An apparatus according to Claim 37,

wherein one of said plurality of groups is arranged in plural subgroups, and

wherein one of the plurality of LMS means corresponding to said one of said plurality of groups comprises at least one LMS means each corresponding to each one of said plural subgroups for providing weighting coefficients.

39. A method for filtering a signal comprising the steps of:

a) receiving an input signal;

b) multiplying the input signal received in step (a) by a first coefficient;

c) delaying the input signal received in step (a) by a first time delay;

d) multiplying a signal from step (c) by a second coefficient;

e) adding a signal from step (b) to a signal from step (d)

f) delaying a signal received in step (c) by a second time delay, wherein the first time delay is different than the second time delay;

g) multiplying a signal from step (f) by a third coefficient; and

h) adding a signal from step (e) to a signal from step (g).

40. A method for filtering a signal comprising the steps of:

a) receiving an input signal;

b) multiplying the input signal received in step (a) by a first coefficient;

c) delaying a signal from step (a) by a first time delay;

d) multiplying a signal from step (c) by a second coefficient;

e) delaying a signal from step (d) by a second time delay, wherein the first time delay is different than the second time delay;

f) adding a signal from step (b) to a signal from step (e)

g) multiplying the signal from step (c) by a third coefficient;

h) delaying a signal in step (g) by the second time delay; and

i) adding a signal from step (h) to the signal from step (d).

41. A method according to Claim 39 or 40, further comprising the step of adjusting the second time delay.

42. A method according to Claim 39 or 40, Further comprising the step of providing a test signal as the input signal.

43. A computer program for filtering a signal comprising the steps of:

a) receiving an input signal;

b) multiplying the input signal received in step (a) by a first coefficient;

c) delaying the input signal received in step (a) by a first time delay;

d) multiplying a signal from step (c) by a second coefficient;

e) adding a signal from step (b) to a signal from step (d)

f) delaying a signal received in step (c) by a second time delay, wherein the first time delay is different than the second time delay;

g) multiplying a signal from step (f) by a third coefficient; and

h) adding a signal from step (e) to a signal from step (g).

44. A computer program for filtering a signal comprising the steps of:

a) receiving an input signal;

b) multiplying the input signal received in step (a) by a first coefficient;

c) delaying a signal from step (a) by a first time delay;

d) multiplying a signal from step (c) by a second coefficient;

e) delaying a signal from step (d) by a second time delay, wherein the first time delay is different than the second time delay;

f) adding a signal from step (b) to a signal from step (e)

g) multiplying a signal from step (c) by a third coefficient;

h) delaying the input signal received in step (g) by the second time delay; and

i) adding a signal from step (h) to the signal from step (d).

45. A computer program according to Claim 43 or 44, further comprising the step of adjusting the second time delay.

46. A computer program according to Claim 43 or 44, further comprising the step of providing a test signal as the input signal.

ABSTRACT

Adaptive Finite Impulse Response Filter control includes structure and steps for receiving an input signal, filtering the input signal with an FIR filter having a plurality of filter stages, and delaying application of the input signal to at least one of said filter stages with respect to the other filter stages to skip filtering a portion of the input signal.

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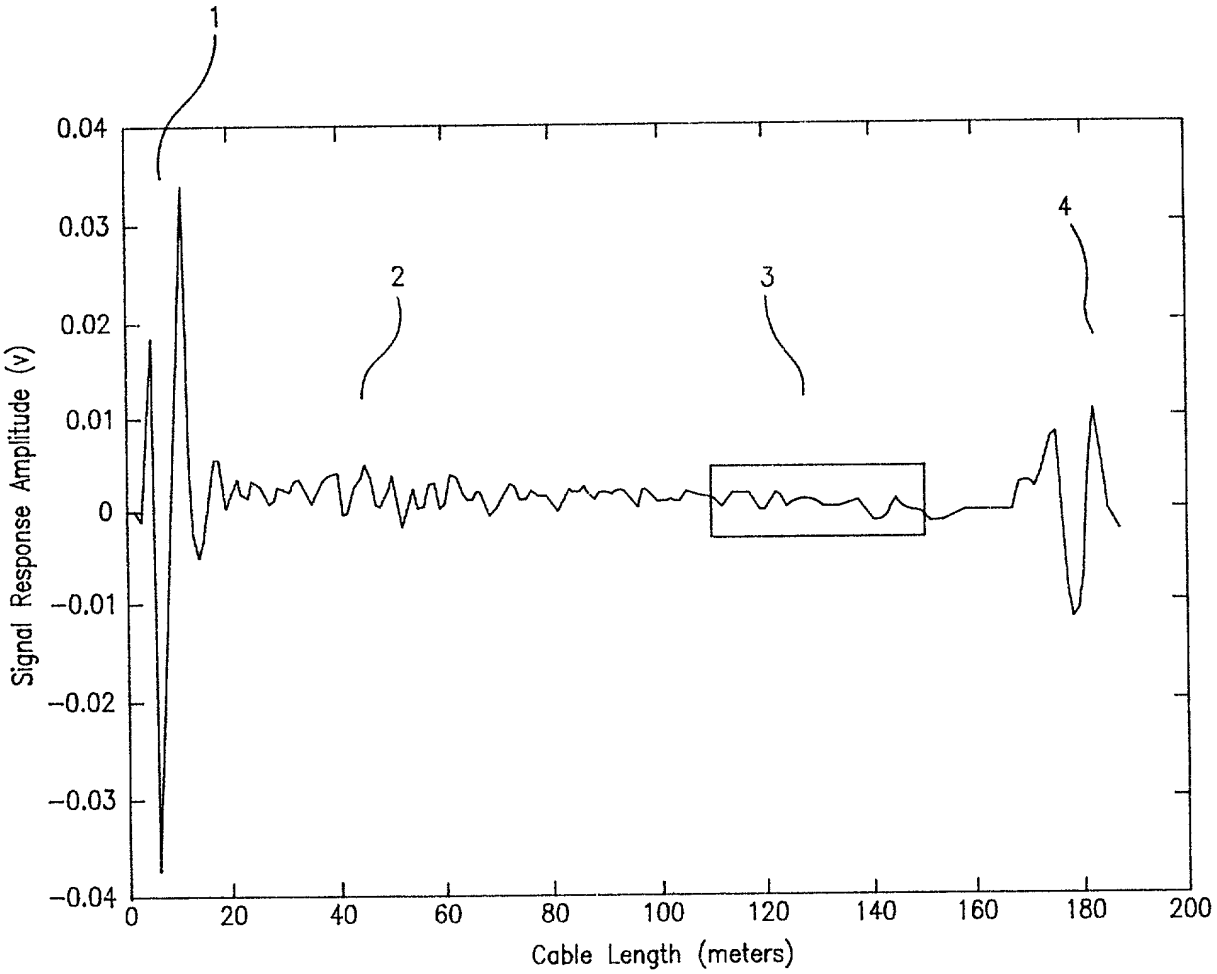
1
2
3
4
0.04
0.03
0.02
0.01
0
−0.01
−0.02
−0.03
−0.04
Signal Response Amplitude (v)
0
20
40
60
80
100
120
140
160
180
200
Cable Length (meters)

FIG. 1

00h00F" 3Z283960

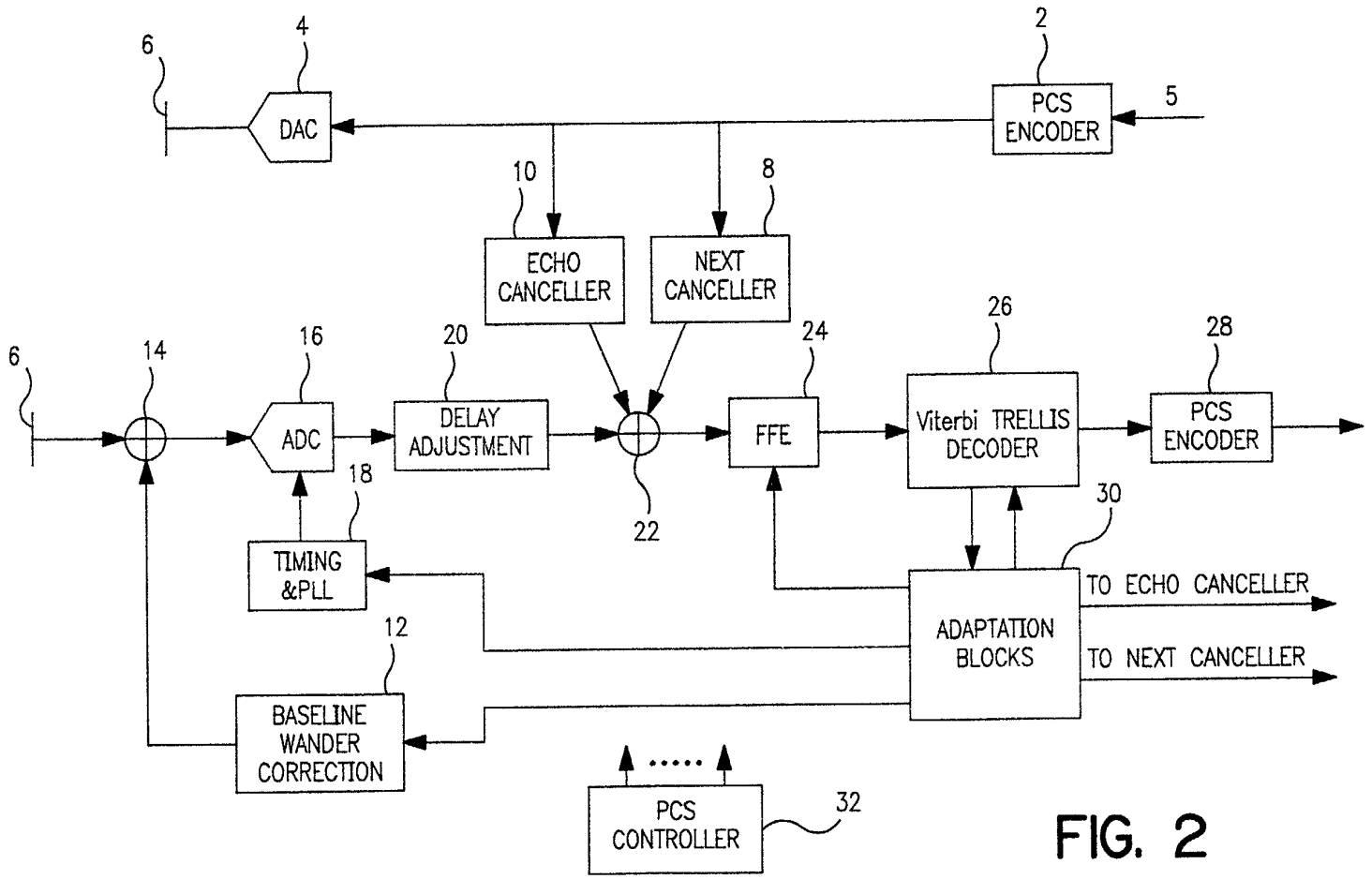

FIG. 2

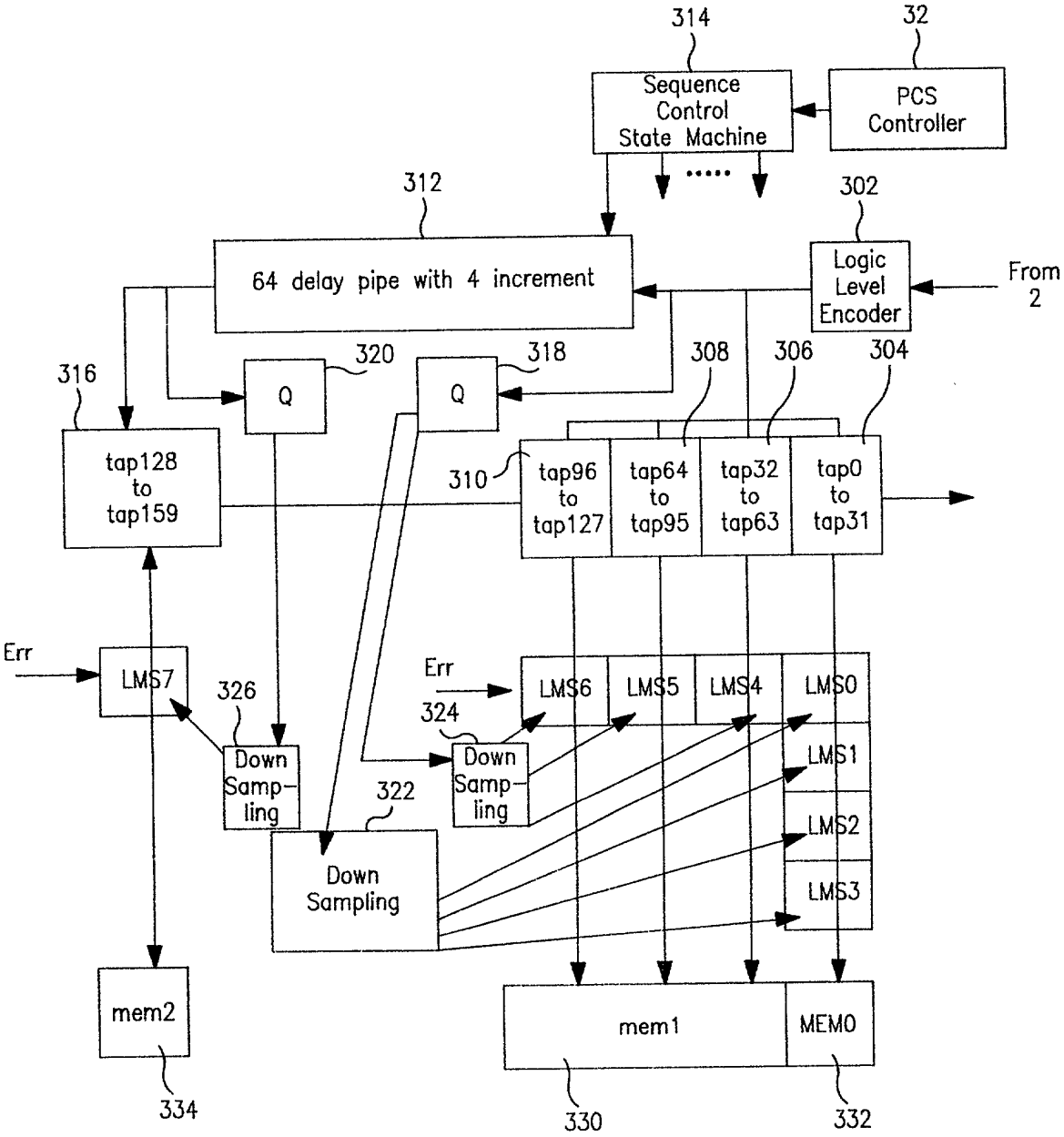
314
32
Sequence Control State Machine
PCS Controller
312
302
64 delay pipe with 4 increment
Logic Level Encoder
From 2
316
320
318
308
306
304
Q
Q
tap128 to tap159
310
tap96 to tap127
tap64 to tap95
tap32 to tap63
tap0 to tap31
Err
LMS7
326
Down Samp-ling
Err
LMS6
LMS5
LMS4
LMS0
324
Down Samp-ling
LMS1
LMS2
LMS3
322
Down Sampling
mem2
mem1
MEM0
334
330
332

FIG. 3

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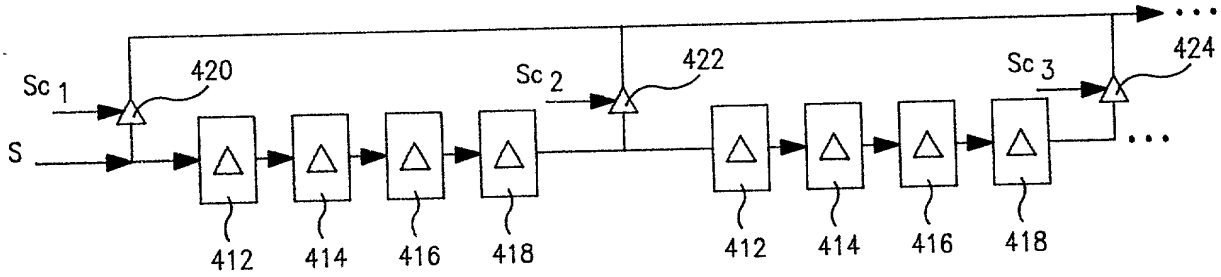

FIG. 4

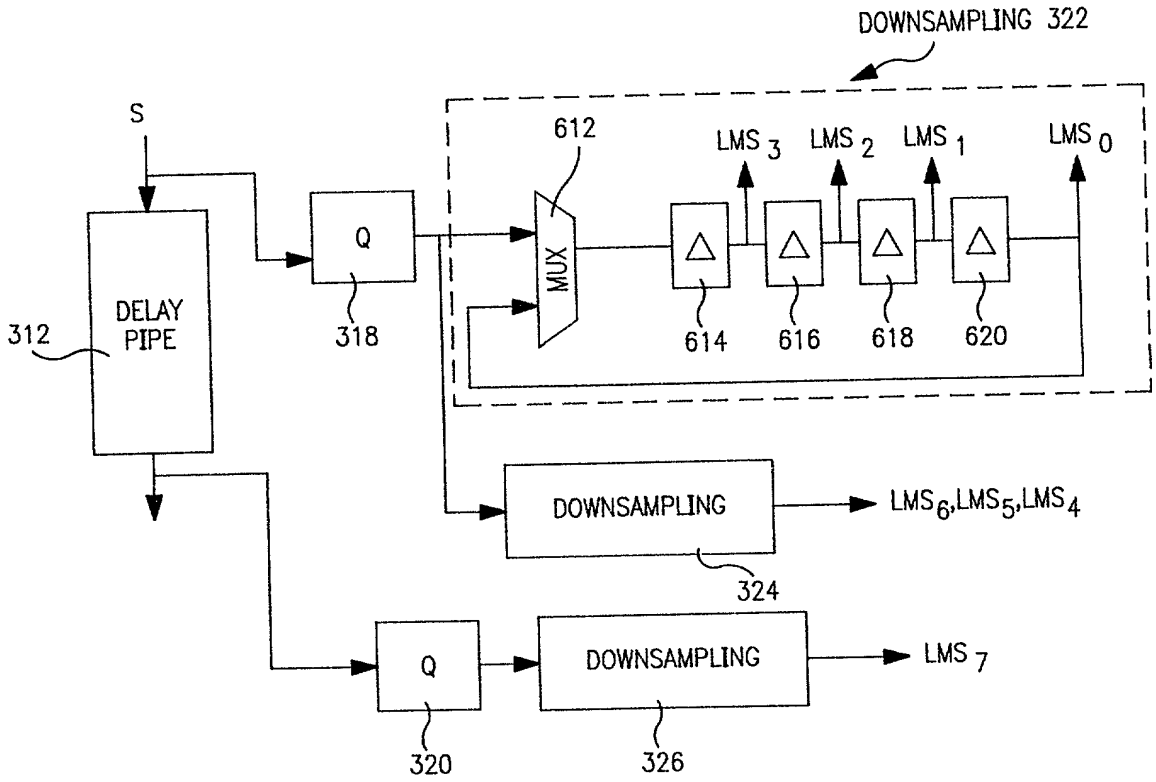

FIG. 6

0040007 "82787960

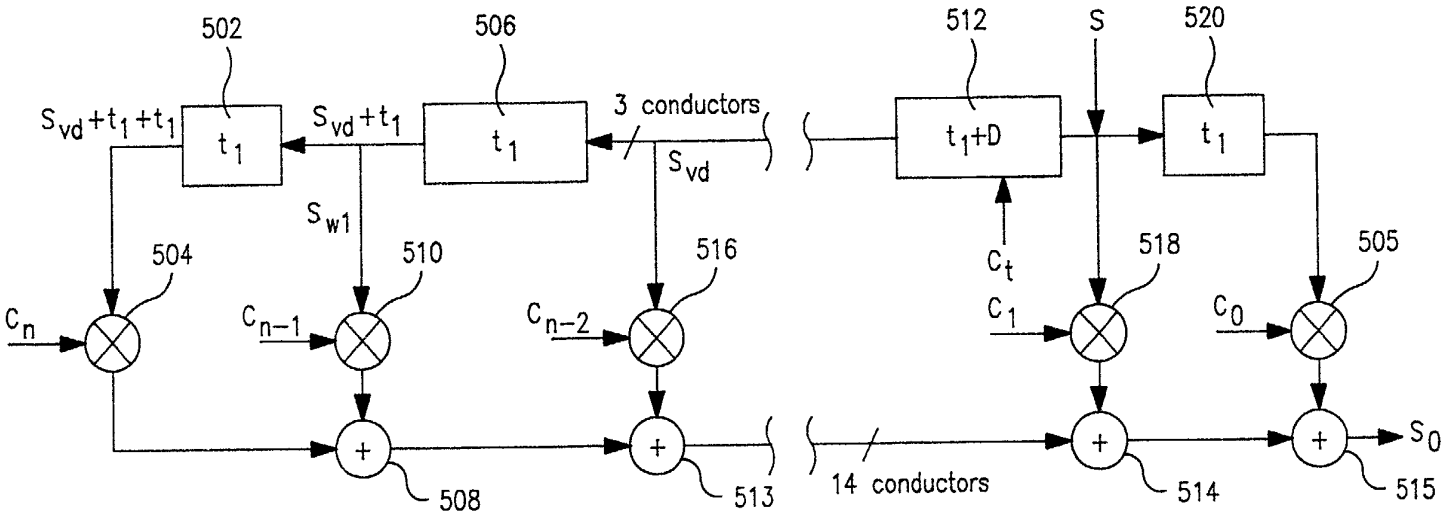

FIG. 5a

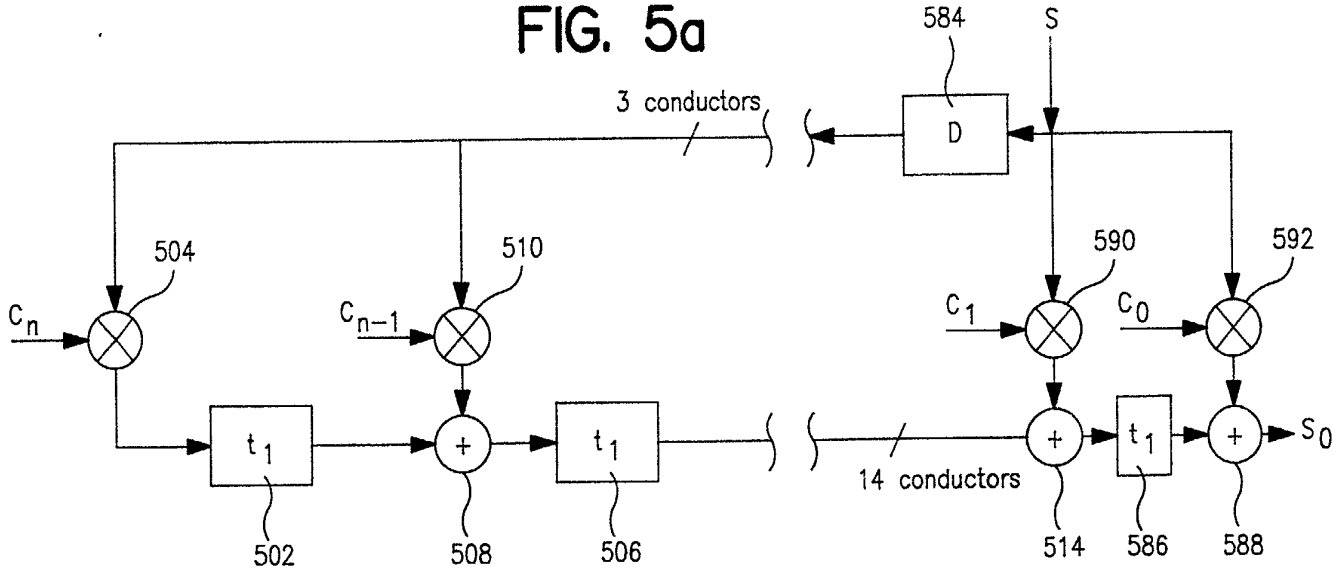

FIG. 5b

0054-0004-US/2005-0350

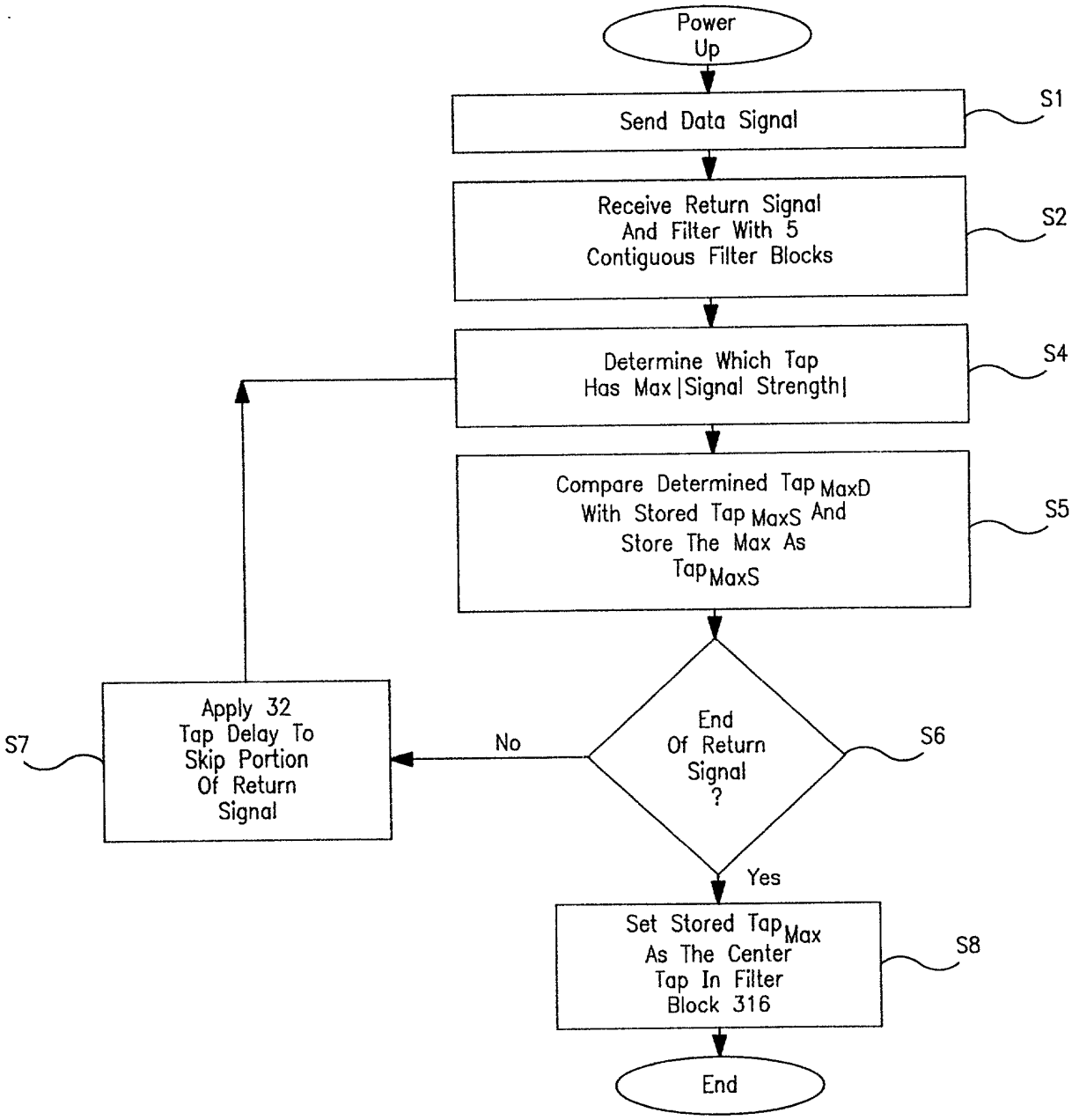

FIG. 7

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(Page 1 of 1)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled MOVABLE TAP FINITE IMPULSE RESPONSE FILTER

the specification of which [X] is attached hereto [ ] was filed on _____ as United States Application No. or PCT International Application No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR §1.56.

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or §365(b), of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application which designates at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed:

Country	Application No.	Filed (Day/Mo./Yr.)	(Yes/No) Priority Claimed

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Application No.	Filed (Day/Mo./Yr.)	Status (Patented, Pending, Abandoned)

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

Application No.	Filed (Day/Mo./Yr.)
60/217,418	July 11, 2000

I hereby appoint the practitioners associated with the firm and Customer Number provided below and Eric B. Janofsky, Reg. No. 30,759, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to the address associated with that Customer Number:

FITZPATRICK, CELLA, HARPER & SCINTO
Customer Number: 05514

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(Page 2)

Full Name of Sole or First Inventor YAT-TUNG LAM

Inventor's signature

Date 10/3/00 Citizen/Subject of HONG KONG

Residence 1103 Oregon Avenue

Palo Alto, California 94303 USA

Post Office Address c/o Marvell Semiconductor, Inc.

645 Almanor Avenue, Sunnyvale, CA 94086

Docket No. 020278-000500